Chapter 4 Field Effect Transistors

1. Introduction

Field Effect Transistors (FETs) are three terminal electronic devices used for varieties of application, mostly similar to BJTs, such as amplifiers, electronic switches and impedance matching circuits. However, the field effect transistor differs from bipolar junction transistor in the following important characteristics.

1. In FETs an Electric Field is established to control the conduction path of output devices without the need for direct contact between the controlling and controlled quantities.
2. Its operation depends upon only the flow of majority carriers, hence, unipolar device.
3. It exhibits high input impedance, typically, in many mega ohms range
4. FET's are less sensitive to temperature variations and because of their construction they are more easily integrated on IC's.
5. FET's are also generally more static sensitive than BJT's.

Basically there are two types of field effect transistors, the ***Junction Field Effect Transistor*** (abbreviated as JFET) and ***Metal-Oxide Field Effect Transistor*** called MOSFET.

2 Junction Field Effect Transistors (JFET)

The basic Structure of junction field effect transistor is formed from a bar of n/p SC material called channel with a region of p/n material embedded in each side (fig. 4.1).Top and bottom of the channel is connected through an ohmic contact to a terminal referred to as, respectively, the drain (D) and source(S).The two embedded regions are electrically connected and form the Gate. In practice, the channel is always lightly doped than the gate.

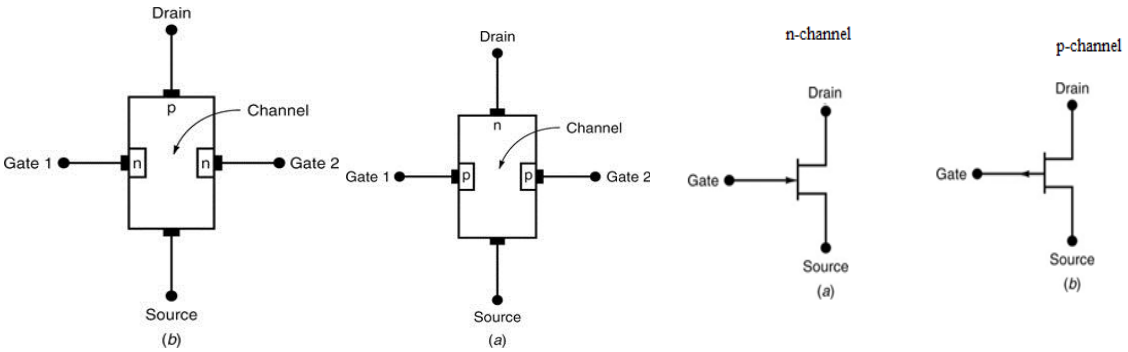


Figure 4.1: Junction Field Effect Transistors basic construction and their symbols

Operating characteristics of JFET

To demonstrate the *i-v* characteristics of JFET lets use the following n-channel JFET circuit layout shown on figure 4.2.For normal operation of JFET the two junctions made between the channel and the two gates should be reverse biased. As can be seen from the circuit diagram there are two possible conditions to control the variation of channel current, either changing the voltage level of V_{GG} or V_{DD}. Depending on this there are two operating conditions.

Case1: $V_{GS} = 0$, V_{DS} increasing to some positive value

Case2: $V_{GS} < 0$ and varying, V_{DS} fixed to some value

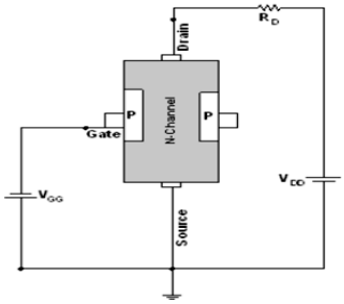


Figure 4.2: i-v characterstics of n-channel JFET

Case1: $V_{GS} = 0$, V_{DS} increasing to some positive value

For a few volts increase in V_{DS}, the current will increase as determined by Ohm's Law.(See fig. 4.3a). But further increase in V_{DS} begins to make the depletion region near the drain to be wider and wider than the source ends because the relative voltage level near the drain is greater than the source. This causes the channel resistance to change. See fig. 4.3(b). As V_{DS} increases and when it gets large enough to cause the two depletion regions touch near the drain ,pinch-off occurs and no further increase in I_D. At this point, I_D maintains the saturation level defined as I_{DSS} and the voltage is called pinch-off voltage V_p. In this region JFETs can act as constant current source. See fig. 4.3(c

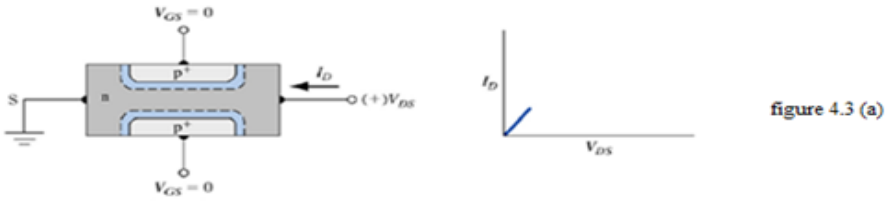
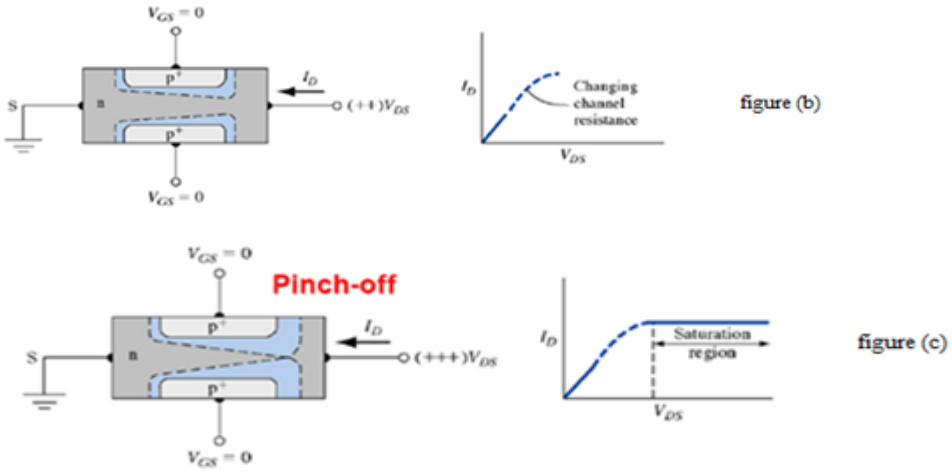
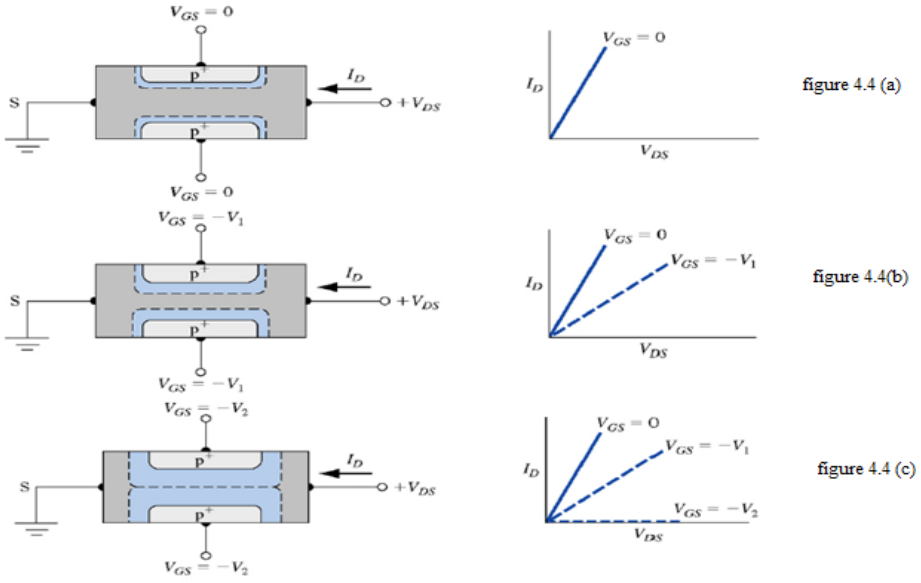


figure 4.3 (a)



Case 2: $V_{GS} < 0$ (V_{GS} varying)

As V_{GS} becomes more negative, the width of the depletion region increases uniformly across the channel causing an increase in channel resistance. See fig. 4.4 (b). At this condition, the effect of varying V_{DS} is to establish depletion regions similar to those obtained with V_{GS}=0V but a lower level of V_{DS} is required to reach the saturation level. If V_{GS} is taken up to a position where the two depletion regions are pinched, then the device will be turned off and any change in V_{DS} will produce no current. See fig. 4.4 (c).



The region to the right of the pinch-off locus on the figure is the region typically employed in linear amplifiers (amplifiers with min distortion of the applied signal) and is commonly referred to as the constant-current, saturation, or linear amplification region. *In the ohmic region JFET can be use as variable resistors of value given as*

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

Where r_o is the resistance of the channel before applying V_{GS} and V_p is the pinch-off voltage

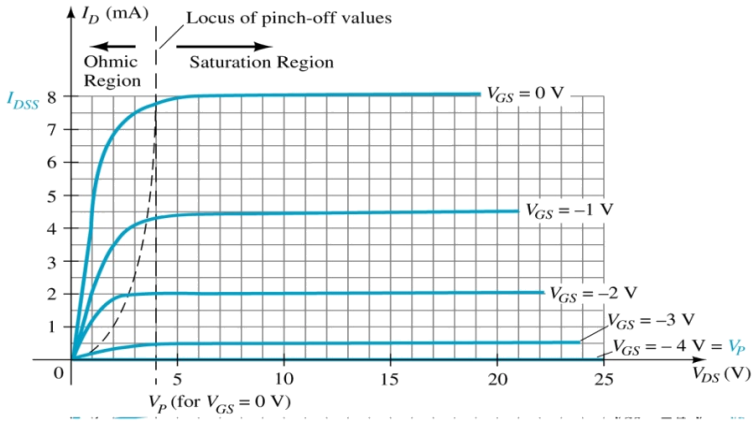


Figure 4.5: current voltage relationships curve

Transfer Characteristics

In a JFET the relationship of V_{GS} (input) and I_D (output) is a little more complicated, and is given by

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(pinchoff)}}\right)\right]^2$$

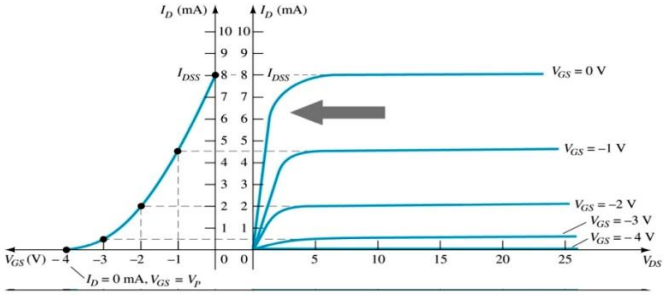


Figure 4.6: transfer charactersitcs curve

3. Metal Oxide Field Effect Transistors

MOSFETs have characteristics similar to JFETs and additional characteristics but they have added features of characteristics extended to the region of opposite polarities of V_{GS} that make them very useful. There are two types: Depletion-Type and Enhancement-Type MOSFET.

3.1. Depletion-Type MOSFET Construction

Figure 4.7 shows the basic construction of n-channel depletion type MOSFET. The Drain (D) and Source (S) are connected to the n-doped regions. These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

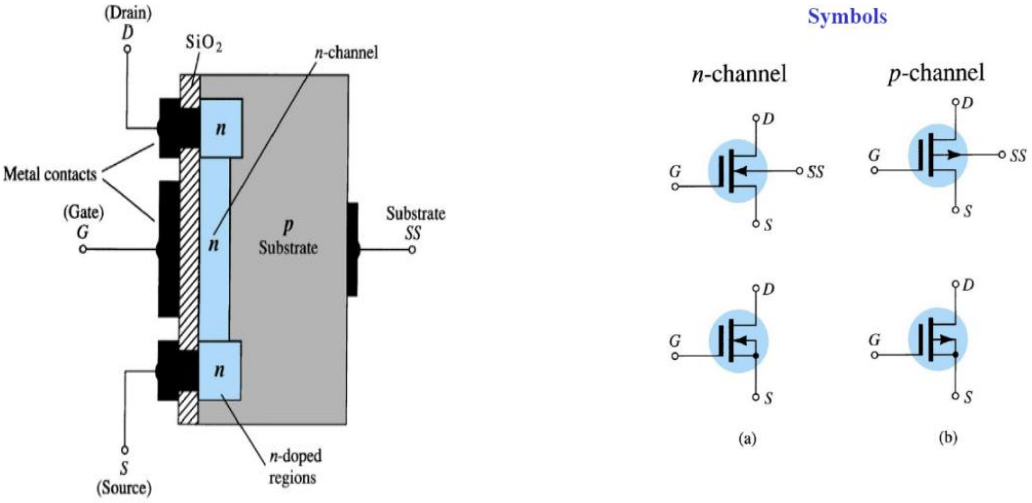


Figure 4.7: Construction of n channel Depletion type MOSFET

Operational Characteristics of Depletion-type MOSFET

Consider the circuit given in the figure 4.8. If the V_{GS} is set to zero and V_{DS} is made to increase, the effect will be to establish a current similar to that established through the channel of the JFET. But if V_{GS} is increase negatively, it will tend to pressure electrons toward the p-type substrate and attract holes from the p-type substrate as shown in Fig. 4.8. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown. This is called depletion mode operation.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction. This is called enhancement mode operation.

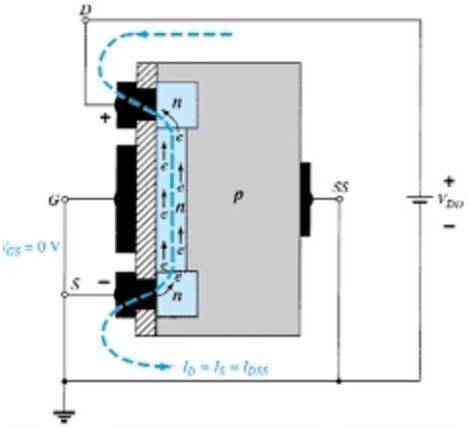


Figure 4.8:Operation of depletion type MOSFETs

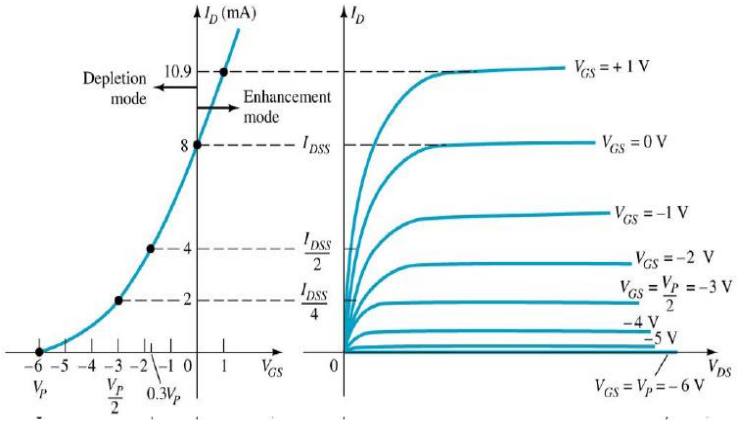
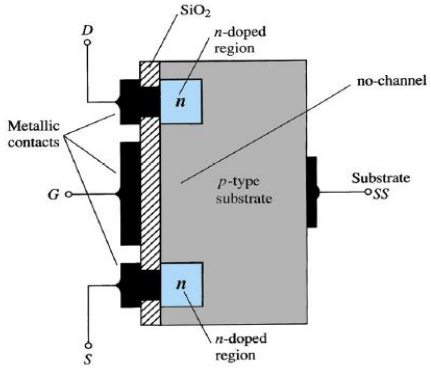
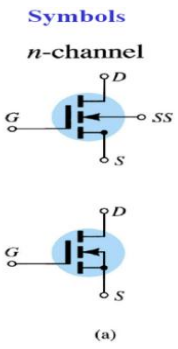


Figure 4.9: Characteristics of n-channel

3.2 Enhancement-Type MOSFET Construction

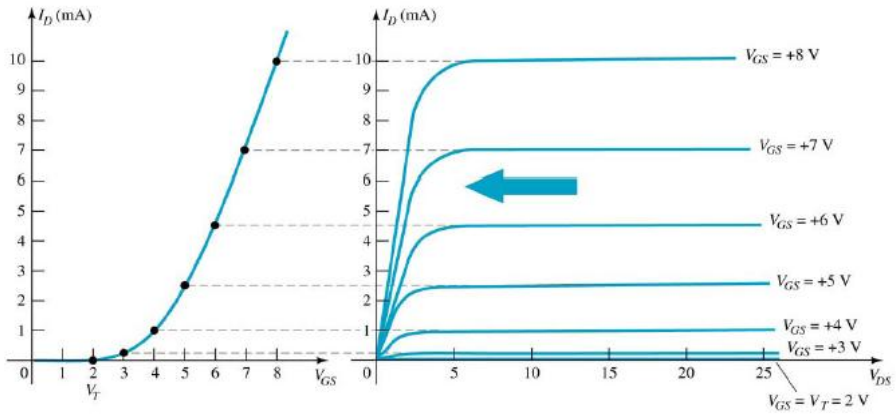
The Drain (D) and Source (S) connect to the n-doped regions. The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO2. There is no channel. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.





Basic Operation

The Enhancement-type MOSFET only operates in the enhancement mode. Hence, V_{GS} is always positive and as V_{GS} increases, I_D increases. But if V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) after the saturation level, V_{DSsat} is reached.



To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

where ,V_T is threshold voltage or voltage at which the MOSFET turns on.

k is a constant that can be determined by using the formula:

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

V_{DSsat} can also be calculated as

$$V_{Dsat} = V_{GS} - V_T$$

P-type FET

The p-channel FET is similar to the n-channel except that the voltage polarities and current directions are reversed. And regarding response time, as electrons are more mobile than holes, there will be considerable delay of current in p-channels compared to n-channel FETs.

MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can establish an unwanted conduction.

Protection:

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage

4. Biasing Techniques

There are different biasing techniques for FET circuits: some of commonly used are fixed bias, self bias and voltage divider bias.

Fixed-bias configuration

Consider the following simplest biasing configuration circuit for the n-channel JFET,

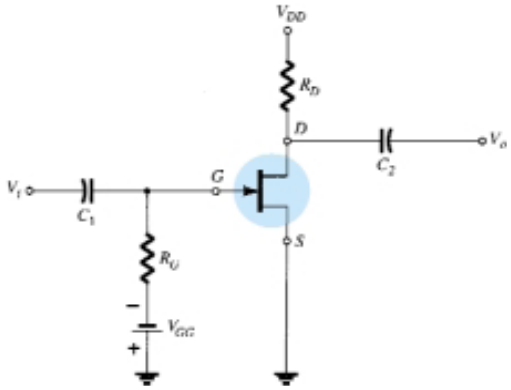


Figure 4.10 Fixed-bias configurations.

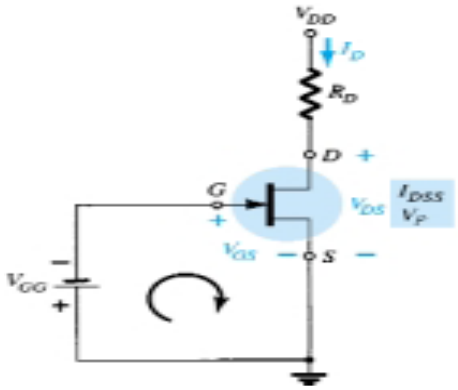


Figure 4.11 Network for dc analysis.

The coupling capacitors (C1 and C2) are open circuits for the dc analysis as is shown in figure 4.11; it would be short circuit for the ac analysis. Attempting the circuit for dc analysis:

$$I_G = \mathbf{0}A \quad and \quad V_{RG} = I_G R_G = \mathbf{0}V$$

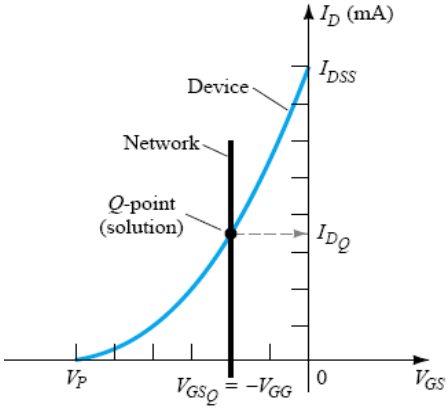
This is shown in the above figure replacing R_G with short circuit.
Applying KVL in the clockwise direction of the indicated loop of Fig. 4.11 will result in

$$-V_{GG} - V_{GS} = 0 \quad and \quad V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration." And the drain current I_D is controlled by:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The level of I_D is simply determined from a vertical line drawn by taking the fixed level of V_{GS} which is superimposed as a vertical line at V_{GS}= - V_{GG}, which is shown in below figure.



Hence, the solution for a fixed bias configuration is the intersection of the two curves in the above figure, and this is commonly referred to as quiescent point or simply Q-point. Note in the figure that the q-point of I_D is determined by drawing a horizontal line across the intersection point of the two curves and crossing the I_D axis.

The drain-to-source voltage of the output section can be determined by applying Kirchhof's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0 \text{ and}$$

$$V_{DS} = V_{DD} - I_D R_D$$

Note from figure 4.12 that, the values of the source, drain, and gate voltages with respect to ground, in relation to V_{DS} and V_{GS} are given by:

$V_S = 0V$ But V_{DS} is given by: $V_{DS} = V_D - V_S$

So $V_D = V_{DS} + V_S$

$V_D = V_{DS}$

In addition, V_{GS} is given by:

$V_{GS} = V_G - V_S \rightarrow V_G = V_{GS} + V_S$

$\therefore \; V_G = V_{GS}$

Self-bias configuration

Here a resistor R_S is introduced in the source leg of the configuration, which is used to determine the controlling gate-to-source voltage (V_{GS}). This is shown in the following figure.

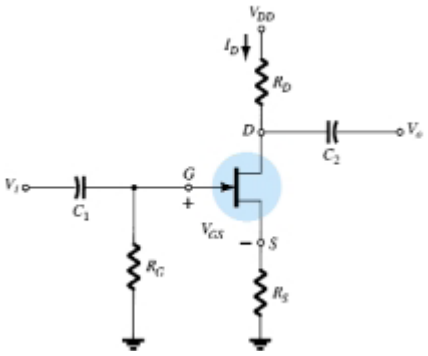


Figure 4.12 JFET self-bias Configuration.

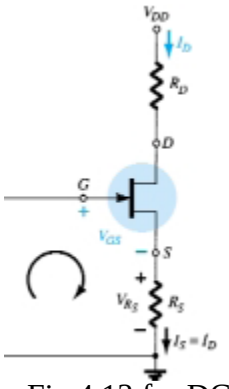


Fig.4.13.for DC analysis.

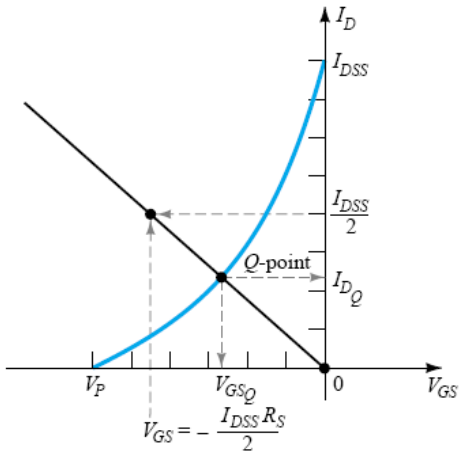
Replacing the capacitors (C1 and C2) with open circuit and R_G with short circuit (since I_G=0A), will result in the network of dc analysis shown in figure 4.13 above.
The current through R_S is the source current I_S, but I_S= I_D and
$V_{R_S} = I_D R_S$. For the indicated loop of figure 4.12,

$$-V_{GS} - V_{R_S} = 0$$
$$V_{GS} = -V_{R_S} = -I_D R_S$$

Note in this case that V_{GS} is a function of the output current *ID* and not fixed in magnitude as occurred for the fixed-bias configuration. The solution of a self bias configuration is obtained by substituting V_{GS} into the drain current equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Solving this quadratic equation will result in appropriate solution of I_D. The graphical analysis can also be used to determine the operating point, which is the intersection point of the device characteristic curve and a straight line curve drawn using the equation $V_{GS} = -I_D R_S$, as shown in the following figure.



Applying Kirchhof's voltage law to the output circuit, the level of V_{DS} can also be determined:

$$V_{DS} + V_{R_S} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D, \qquad but\ I_S = I_D$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

In addition,

$$V_S = I_D R_S, \qquad and \quad V_G = 0V$$
$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

Voltage Divider Bias Configuration

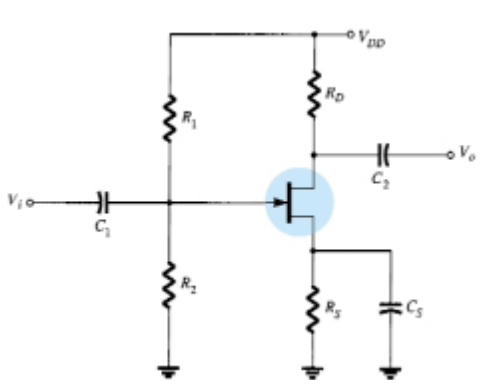


Figure 4.14 Voltage-divider bias arrangements.

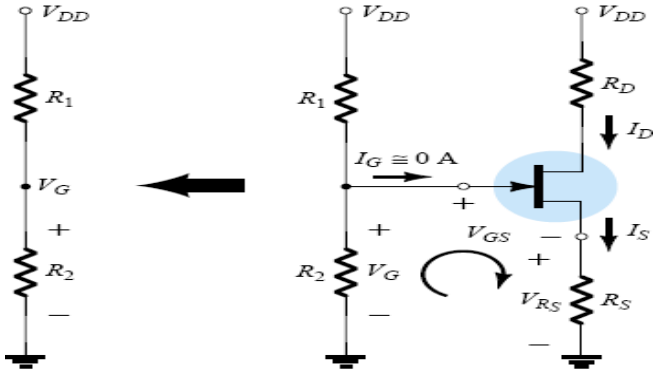


Fig.4.15. For dc analysis

As shown in Fig.4.15, all the capacitors are replaced with open circuit and the voltage V_{DD} is separated in to two equivalent sources, which split the input and output regions of the network. And since $I_G = 0$A, R_1 and R_2 are in series and this will result in V_G to be equal with V_{R2}.

Now the voltage V_G is given by using voltage divider rule:

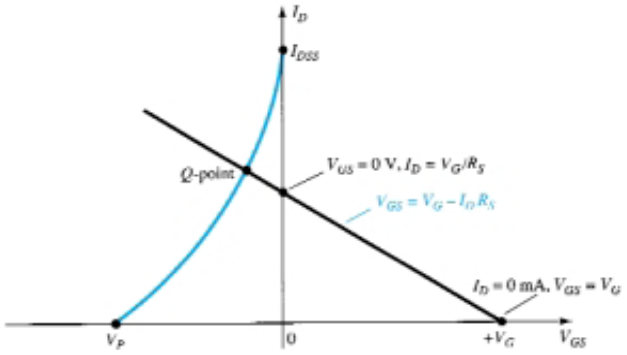
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhof's voltage law in the clockwise direction for the indicated loop of Fig. 4.15:

$$V_G - V_{GS} - V_{R_S} = 0, \qquad and \quad V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we get: $V_{GS} = V_G - I_D R_S$

This is an equation of a straight line, and the intersection point of this curve with the device transfer curve will result in the operating point and the corresponding levels of I_D and V_{GS}. It looks like the following figure:



Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner.

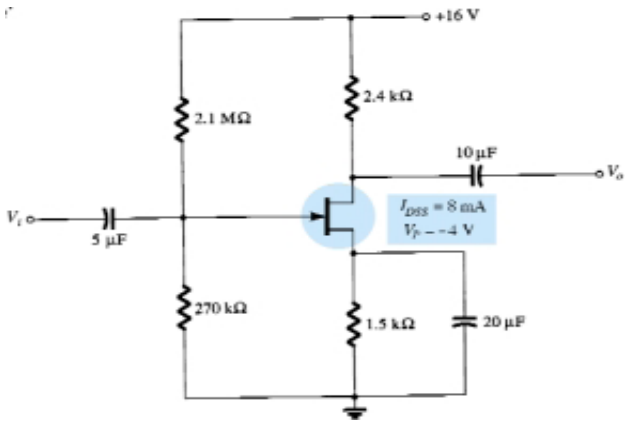
That is, $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Example 4.1: Determine I_{DQ} and V_{GSQ}, V_D, V_S, V_{DS}, and V_{DG} for the following for circuit



Solution:

To determine the operating point, first find the intercepts on the I_D and V_{GS} axes on which the straight line passes.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{270K\Omega(16V)}{2.1M\Omega + 270K\Omega} = 1.82V$$

$$V_{GS} = V_G - I_D R_S$$

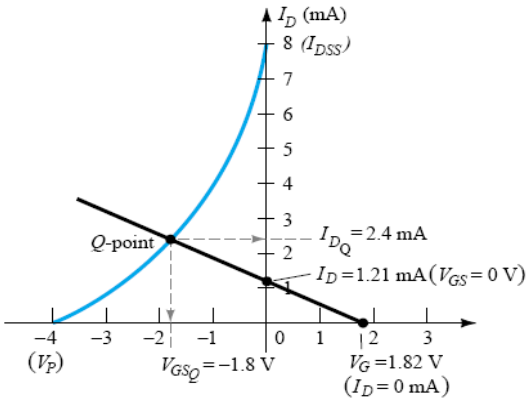
$$= 1.82V - I_D\,(1.5K\Omega),$$

$when\ I_D = 0A$: $V_{GS} = 1.82V$

$when\ V_{GS} = 0V$: $I_D = \frac{V_G}{R_S} = \frac{1.82V}{1.5K\Omega} = 1.21mA$

The intersection point of this line and the transfer curve gives us the Q-point as shown below:

I_{DQ} = 2.4mA and V_{GSQ}= - 1.8V.This can also be determined using the quadratic equation obtained by substituting the value of V_{GS} into the i-v characteristics equation.



$V_D = V_{DD} - I_D R_D$ = 16V- 2.4mA (2.4KΩ) =**10.24V**

$V_S = I_D R_S$ = (2.4mA)(1.5KΩ) = **3.6V**

$V_{DS} = V_{DD} - I_D(R_S + R_D)$ or $V_{DS} = V_D - V_S = 10.24 - 3.6 = 6.64V$

$= 16V - 2.4mA(1.5K + 2.4K) = 6.64V$

The voltage V_{DG} is easily determined by:

$V_{DG} = V_D - V_G = 10.24 - 1.82 = 8.42V$

5. Small-Signal FET model

The small-signal h-parametric model of FET is represented as in the figure 4.16.

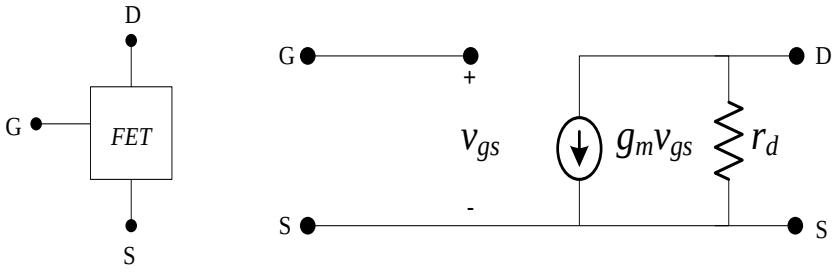


Figure 4.16 FET small signal model

Input impedance (r_i)

As the gate current (I_G) is nearly zero, we can assume the input impedance of FET to be very large.

$$r_i = \frac{\partial V_{GS}}{\partial I_G}\Big|_{V_{DS}=Const} \approx \infty \rightarrow open\ circuit$$

Trans-admittance or Trans-conductance(g_m)

<u>For JFET's</u>

$$g_m = (\partial I_D)/(\partial V_{GS}) \ | @\ Q-point$$

$$g_m = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1 - {V_{GS}}/{V_P}\right)\right]^2 = \frac{2\,I_{DSS}}{|V_P|}\left[1 - {V_{GS}}/{V_P}\right], \text{ let}$$

$$g_{m0} = \frac{I_{DSS}}{|V_P|}$$

$$\therefore\ g_m = 2g_{m0}\left[1 - {V_{GS}}/{V_P}\right]$$

<u>For MOSFET's</u>

$$g_m = \frac{\partial}{\partial V_{GS}}[K\,(V_{GS} - V_T)]^2 = 2K[V_{GS} - V_T]$$

Output impedance (r_d)

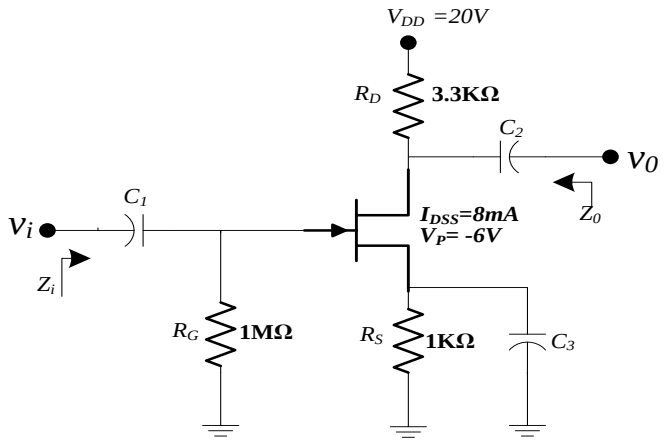
$$r_d = \frac{1}{y_{os}} = \frac{\partial V_{DS}}{\partial I_D}\Big|_{V_{DS}=constant}$$ *, where y_{os} is defined as the output-admittance of the transistor*

Example 1

For the self-bias n-channel JFET shown in the following figure, calculate the

a) *input and output impedances*

b) *voltage gain. Assume,* $y_{os}=20\mu S$



DC Analysis;

$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$, *but from loop 1*, we get $V_{GS} = -R_S I_D$

$$I_D^2 + \frac{V_P}{R_S}\left(2-\frac{V_P}{I_{DSS}R_S}\right)I_D + \frac{V_P^2}{R_S^2} = 0 \rightarrow I_D^2 + \frac{-6}{1k}\left(2-\frac{-6}{8mx1k}\right)I_D + \frac{(-6)^2}{(1k)^2} = 0$$

$$\rightarrow I_D^2 - 16.5I_D + 36 = 0 \rightarrow I_{D1} = 2.6mA \text{ or } I_{D2} = 14mA ,$$

Since $I_{D1} < I_{DSS}$, $\rightarrow I_{DQ} = 2.6mA$

From loop 2, $V_{DSQ} = V_{DD} - I_{DQ}(R_S + R_D) \rightarrow V_{DS} = 20 - 2.6m(3.3k + 1k) = 8.82V$

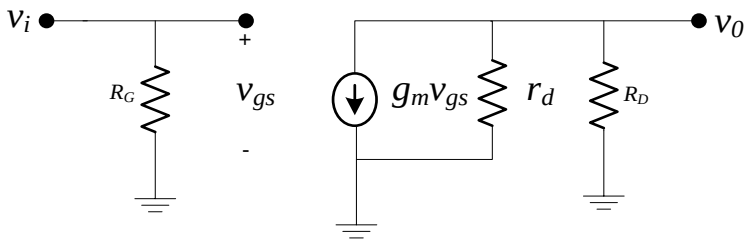
And $V_{GS} = -R_S I_D = -1kx2.6m = -2.6V$

AC Analysis

$$g_m = \frac{2\,I_{DSS}}{|V_P|}\left[1 - {V_{GS}}/{V_P}\right] = \frac{2x8m}{|-6|}\left[1 - \frac{-2.6}{-6}\right] = \boldsymbol{1.51mS}$$

Ac equivalent circuit

Shorting all DC sources and capacitors



a) *Input impedance,*

$$Z_i = R_G = \mathbf{1}M\Omega \ ,$$

b) *Output impedance,*

$$z_o = R_D \| r_d = 3.3K\Omega\left(\frac{1}{20\mu S}\right) = 3.3K\Omega$$

c) *Voltage gain,*

$$A_V = \frac{V_O}{V_{in}} = \left(-g_m R_D \| r_d\right) = -1.5mS\,x\,3.3K\Omega \| 50K\Omega = -4.98$$